REMARKS

Claims 1-6, 12-18, and 31-34 are all the claims presently listed in the application. Claims 7-11 and 19-30 are cancelled as addressing a non-elected invention. New claims 31-34 are added.

As best understood, the Examiner considers that claims 1-6 and 12-18 are pending, and, presumably, therefore, claims 7-11 and 19-30 are withdrawn. It is noted that the Office Action Summary lists claim 6 as also withdrawn.

It is noted that Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicants gratefully acknowledge the Examiner's indication that claims 2, 3, 13, and 14 would be allowable if rewritten in independent format. However, Applicants believe that all the claims are allowable over the prior art currently of record.

Claims 1, 5, 12, and 17 stand rejected under 35 USC §102(b) as anticipated by US Patent 5,888,883 to Sasaki et al. Claims 1, 4, 12 15, and 16 stand rejected under 35 USC §102(e) as anticipated by US Patent 6,805,808 to Fujii et al. Claims 6 and 12 stand rejected under 35 USC §103(a) as unpatentable over Fujii.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

In one aspect, as described, for example in claim 1, the present invention is directed to a method of producing a plurality of semiconductor elements by individually dividing the semiconductor elements formed on a substrate. Semiconductor layers are removed on parting lines so that (i) only an electrode-forming layer on a side near the substrate remains or (ii) no semiconductor layers remains on the parting lines. A protective film is formed so that the semiconductor layers are covered with the protective film and the protective film can be removed by an after-process. The substrate is scanned with a laser beam along the parting lines to form separation grooves in a front surface of the substrate. The protective film and unnecessary products produced by the laser beam scanning are removed. The separation grooves formed along the parting lines by the laser beam scanning are used for dividing the

substrate into individual semiconductor elements.

In accordance with a second aspect, the present invention is directed to a method of producing a plurality of semiconductor elements by individually dividing the semiconductor elements formed on a substrate. Semiconductor layers are removed on parting lines so that (i) only an electrode-forming layer on a side near to said substrate remains on said parting lines or (ii) there is no semiconductor layer on said parting lines. The substrate is scanned along the parting lines with a laser beam to thereby form broken line-shaped or dot line-shaped separation grooves. The broken line-shaped or dot line-shaped separation grooves formed by laser beam scanning along the parting lines are used so that the substrate is divided into individual semiconductor elements.

In contrast, as explained beginning at line 15 of page one of the specification, when sapphire, spinel, or the like is used as the substrate material, rather than silicon or gallium arsenide, processing is more difficult, including the division of the material into individual elements.

As explained beginning at line 1 on page 2, the conventional method uses a diamond-bladed dicer to make a half-cut on the front surface and a shallow rear groove on the back surface with a scriber and results in relative poor yield.

As explained beginning at line 9 of page 3, attempting to use a laser beam for the forming separation grooves causes contamination with reaction products, including opaque deposits that reduce the light-extracting efficiency of light emitting elements.

In contrast, the present invention provides a method in which division by a laser beam is facilitated by first etching away appropriate layers of semiconductor layers on the parting lines and then covering the exposed semiconductor layers with a protecting layer that can then be removed after the laser etching, along with any of contaminants produced by the laser etching.

II. THE PRIOR ART REJECTIONS

The Examiner considers that Sasaki and Fujii respectively anticipate various claims of the present invention. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by Sasaki nor Fujii.

The Rejections Based on Sasaki

The Examiner alleges that Sasaki teaches the present invention described by claims 1, 5, 12, and 17, pointing to the description at lines 25-50 of column 1 and, for claim 10, Figure 10.

However, Applicants submit that the description in column 1 fails to satisfy the plain meaning of the claim language of even the independent claims.

That is, relative to claim 1, the plain meaning of the claim language of the first two claim limitations requires that (1) semiconductor layers be removed on parting lines and (2) covering the semiconductor layers prior to using the laser to form separation grooves. Sasaki fails to do either of these two steps.

That is, as clearly described beginning at line 6 of column 2 and shown in Figures 1-5, the protective tape 3 is applied for purpose of protecting the pattern formation surface 1' during the lapping process shown in Figure 2, wherein the bottom surface of the wafer is ground down. In Figure 3 the protective tape is clearly shown as being removed prior to the formation of separation grooves shown in Figure 5 (e.g., assuming that a laser is used to form the separation grooves shown in this figure).

Therefore, contrary to the allegation of the Examiner on page 2 of the Office Action, the prior art shown in Sasaki '883 does not show any removal of semiconductor layers in the parting lines prior to formation of the separation grooves shown in Figure 5. Moreover, Figure 5 of Sasaki clearly fails to show any protective layer used in the formation of the separation grooves.

As explained at lines 13-16 of page 34, this protective film is used to preclude deposition on the semiconductor layers of substrate melted by the laser when the separation groove are formed by laser irradiation. As explained at lines 12-25 of page 3, the method of laser cutting in the prior art has the problem of causing the melted substrate material from falling back onto the semiconductor layers or light-emitting elements as contaminant deposits.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Saski of: "...removing semiconductor layers on parting lines so that (i) only an electrode-forming layer on a side near said substrate remains or (ii) no semiconductor layers remains on said parting lines; forming a protective film so that said semiconductor layers are covered

with said protective film and said protective film can be removed by an after-process ....", as required by claim 1. Therefore, claims 1 and 5 are clearly patentable over Saski.

Relative to claims 12 and 17, the Examiner points to lines 30-35 of column 1 as demonstrating the formation of separation grooves that are broken line-shaped or dot line-shaped grooves, such as are exemplarily shown in the embodiment described beginning at line 18 on page 48 and shown in Figure 11.

Applicants submit that lines 30-35 of column 1 of Sasaki make no suggestion whatsoever about forming separation grooves that are discontinuous grooves defined by the concept of "broken line-shaped"or "dot line-shaped" grooves.

Hence, turning to the clear language of the claims, in Sasaki there is no teaching or suggestion of: "...scanning said substrate along said parting lines with a laser beam to thereby form broken line-shaped or dot line-shaped separation grooves ....", as required by independent claim 12.

Therefore, claims 12 and 17 are clearly patentable over Sasaki.

The Rejections Based on Fujii

The Examiner alleges that Fujii '808 anticipates the present invention defined by claims 1, 4, 12, 15, and 16, and renders obvious the present invention defined by claims 6 and 18. To support the rejection for independent claims 1 and 12, the Examiner points to Figures 2(a) through 2(f) and is understood as relying upon resist layer 5 as satisfying the claim limitation that a protective layer is deposited to protect the semiconductor layer 3 during the groove formation shown in Figure 2(c).

Applicants submit that the Examiner's interpretation of the process in Fujii is somewhat confused, perhaps in no small part due to what appears to be several mistakes in the layout of the figures in Fujii. That is, Applicants submit that one having ordinary skill in the art would recognize that Figure 2(d) clearly indicates the condition of the wafer after the diamond layer has been polished, as described at lines 53-58 of column 3. Applicants also submit that the description of the resist layer 5 in lines 61-64 of column 3 actually means that the resist layer 5 is used in the photolithographic technique to form the SAW filter elements 3 by serving as an etching layer to form the SAW filter elements 3. That is clear by

recognizing that the resist layer 5 aligns with the SAW filter elements 5. It is further noted the description in column 1 does not provide any reason to add a protective layer after the photolithographic process mentioned in lines 61-64.

Therefore, Applicants submit that the resist layer 5 is not added after removing semiconductor layers on the parting lines, as required by the plain meaning of the claim language. Moreover, Applicants submit that, even if the resist layer 5 shown in Figure 2(c) had been added after the step of removing the semiconductor layer 3 on parting lines, this resist layer would protect only the top surface of semiconductor layer 3. The sides of the semiconductor layer 3 would still be subject to contamination from the melted materials. Fujii simply fails to account for possible contamination of the SAW filter elements 3 during the lasing operation for forming the separation grooves.

In contrast, as shown in Figure 1B of the present Application, the technique of the independent claims clearly describes that the semiconductor layers are first removed from the parting lines regions A and then a protective layer 4 is deposited for protection of the layers 3p and 2n during the laser operation.

Applicants submit that there is no indication that resist layer 5 of Figure 2(c) of Fujii was formed after the semiconductor layer 3 was etched away for the parting lines. Moreover, it is also clear that the sides of the semiconductor layer 3 will not be protected from contamination of the laser operation to form the front-side separation grooves 6.
Hence, turning to the clear language of the claims, there is no teaching or suggestion in Fujii to: "... removing semiconductor layers on parting lines ... ; forming a protective film so that said semiconductor layers are covered with said protective film and said protective film can be removed by an after-process ....", as required by independent claim 1.

Relative to the rejection for claim 12, Applicants submit that the description at lines 45-50 of column 1 do not suggest the discontinuous groove lines described in the claim.

Hence, turning to the clear language of the claims, in Fujii there is no teaching or suggestion of: "...scanning said substrate along said parting lines with a laser beam to thereby form broken line-shaped or dot line-shaped separation grooves ....", as required by independent claim 12.

Therefore, Applicants submit that claims 1, 4, 12, 15, and 16 are clearly patentable over Fujii.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggested by Sasaki or Fujii, and the Examiner is respectfully requested to reconsider and withdraw these rejections based on Sasaki and on Fujii.

III. FORMAL MATTERS AND CONCLUSION

It is noted that the Office Action Summary states that a one-month response is required for responding to the Office Action mailed on July 20, 2006. In a telephone interview with the Examiner on July 25, 2006, the Examiner acknowledged that this one-month response deadline was incorrect and that the normal three-month response deadline applied.

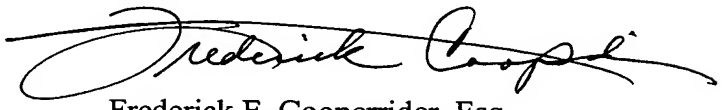
In view of the foregoing, Applicants submit that claims 1-6, 12-18, and 31-34, all the claims pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 10/13/06



Frederick E. Cooperrider, Esq.
Registration No. 36,769

McGinn Intellectual Law Group, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254